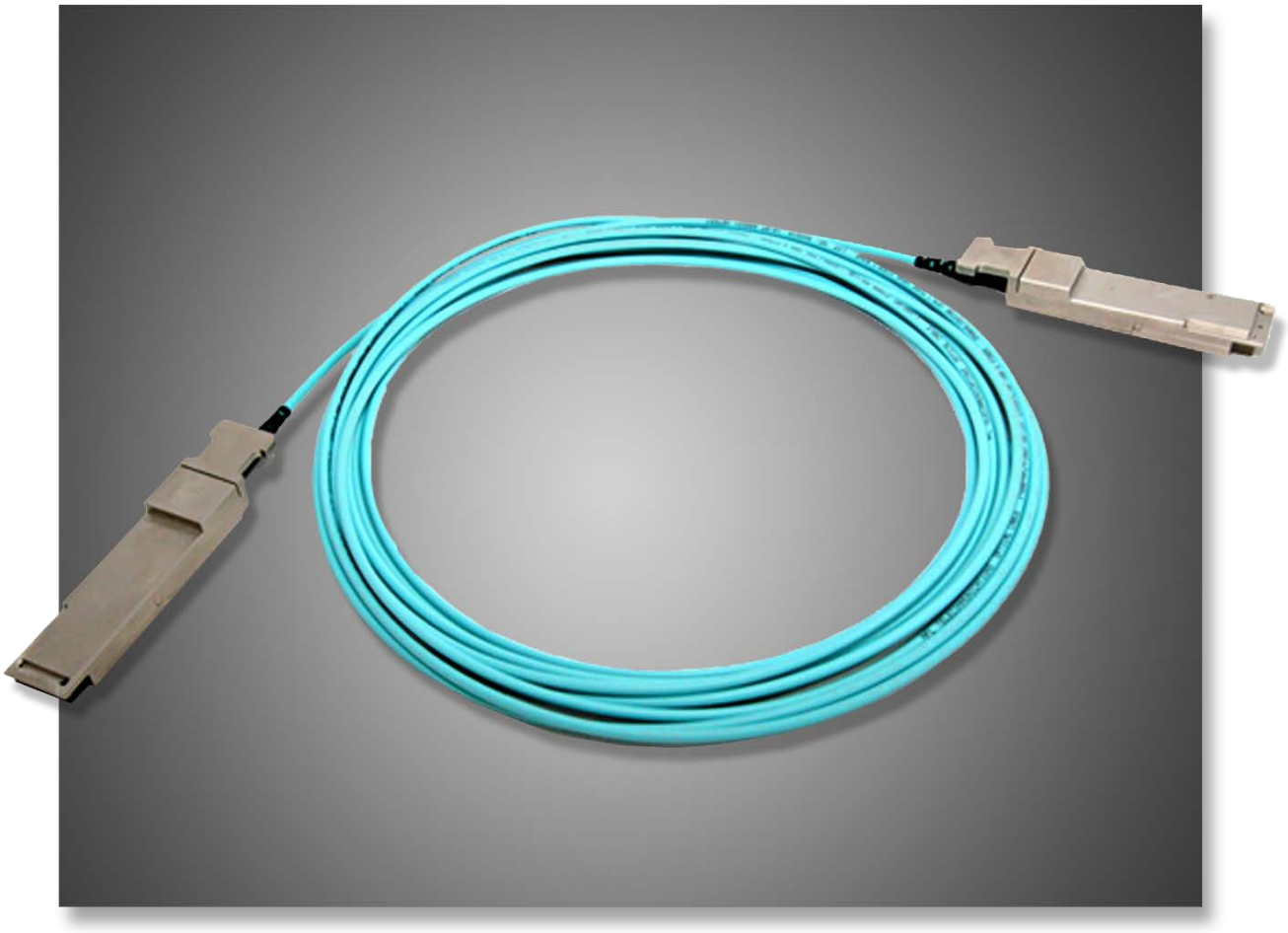
40 Gbps
QSFP+ ACTIVE OPTICAL CABLE ASSEMBLY
User Manual



Covering:
QSFPO -40G Series

November 2012

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INTRODUCTION

QSFPO-40G Series

The QSFPO-40G AOC is a 4-channel active optical cable assembly for QSFP+ applications that is designed to meet the QSFP+ 10Gbs x4 Pluggable Transceiver SFF-8436 specification. This full-duplex optical assembly offers 4 independent transmit and receive channels, each capable of 10Gbps for an aggregate bandwidth of 40Gbps. The cable uses standard multimode fiber cable carrying a nominal wavelength of 850nm. The electrical interface is a standard QSFP+ 38 contact edge type connector and is electrically compliant with the SFI+ and PPI interface supporting Infiniband, Ethernet, Fiber Channel and other protocols. The connector is hot pluggable and provides I^2C serial access via an on-board microcontroller.

Figure 1: QSFPO Active Optical Cable

The QSFPO comes pre-tested and can be used as a direct replacement for traditional copper cables but with the added benefit of a lighter weight and smaller diameter solution for cable lengths from 1 to 100 meters. It can also be used to replace a pair of transceivers proving equivalent performance at a lower cost.

Product Features

- 4 high-speed full duplex channels
- 40Gbs QSFP+ compatible
- SFI and PPI electrical interface compliant
- Supports Ethernet 40 GbE
- Supports Ethernet 10 GbE
- Supports Infiniband QDR, DDR, and SDR
- Infiniband Approved Integrators List
- Cable lengths from 1 to 100 meters
- Small 3mm diameter fiber cable
- Low power consumption: 0.6W typical at room temperature, 0.8W typical at 75°C
- Bit Error Rate better than 10^{-15} (100m cable length)
- 0 to 70°C Operating case temperature range
- Proven high reliability 850nm VCSEL technology
- Two Wire Serial (TWS) interface with maskable interrupt

Applications

The QSFPO-40G active optical cable complies with the standard for Infiniband QDR and Ethernet 40 GbE (40 Gigabit Ethernet) applications and is listed on the Infiniband Trade Association's Approved Integrators List for lengths from 1 to 100 meters.

The cable ends are electrically compliant with the SFI+ and PPI interface and capable of supporting Infiniband, Ethernet, as well as Fiber Channel and other protocols. The cable is hot pluggable, and provides a standard I^2C serial digital control interface via an on-board micro-controller.

The QSFPO-40G active optical cable assembly is ideal for High Performance Computing, Data Center, Storage Area Network, Telecom Switched Network, and is a direct replacement for copper cables where bandwidth, distance and/or cable density needs to be optimized.

FUNCTIONAL DESCRIPTION

The QSFPO AOC has a miniature optical engine embedded into each end of the cable assembly. The engines interconnect 4 independent transmit / receive lanes. An on board micro-controller provides control, diagnostic and monitoring for the cable functions, as well as the external I^2C serial communication interface.

A functional block diagram of the engine is shown in Figure 2. The transmitter section consists of a 4-channel VCSEL (Vertical Cavity Surface Emitting Laser) array, a 4-channel input buffer and laser driver. The receiver section consists of a 4-channel PIN photodiode array, a 4-channel TIA array, and a 4-channel output buffer.

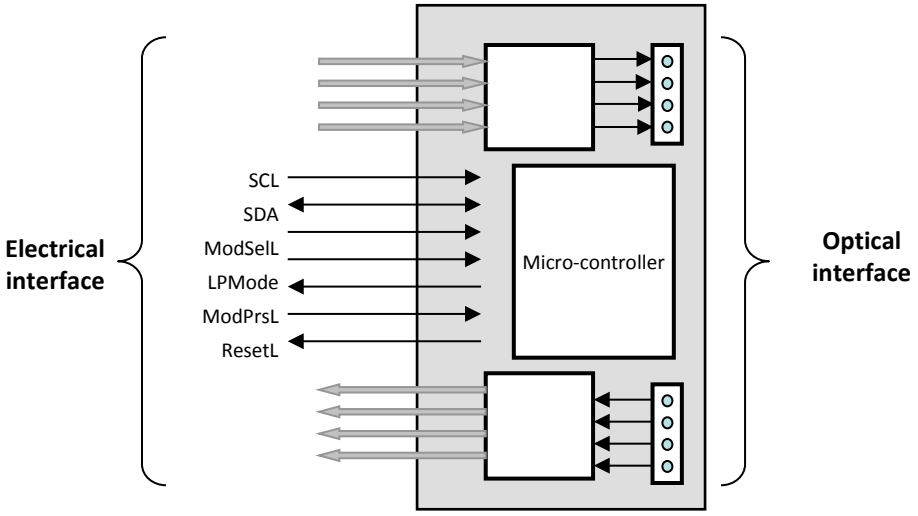


Figure 2: Transceiver Functional Block Diagram

Transmitter Block

The optical transmit portion of the engine incorporates a 4-channel VCSEL (Vertical Cavity Surface Emitting Laser) array, a 4-channel input buffer and laser driver, diagnostic monitors, control and bias blocks. The transmit input buffer provides CML compatible differential inputs presenting a nominal differential input impedance of 100 Ohms. AC coupling capacitors are located on the Optical Engine board and are not required on the host board. An LVTTL compatible Two Wire Serial (or I^2C) interface is provided for module control and diagnostics. Status, alarm and fault information are available via the TWS interface. To reduce the need for polling, a hardware interrupt signal is provided to inform hosts of an assertion of an alarm, Loss of Signal (LOS) and Transmitter (Tx) fault.

Receiver Block

The optical receiver portion of the engine incorporates a 4-channel PIN photodiode array, a 4-channel TIA array, a 4 channel output buffer, diagnostic monitors, control, and bias blocks. The Receiver Output Buffer provides CML compatible differential outputs for the high speed electrical interface presenting nominal single-ended output impedances of 50 Ohms to AC ground and 100 Ohms differentially that should be differentially terminated with 100 Ohms. AC coupling capacitors are located on the Optical Engine and are not required on the host board.

Management Interface

The internal optical engine provides digital diagnostics and control/monitor functions, as specified in SFF-8436. A micro-controller, which can be accessed through the 2-wire interface, monitors and reports this information. The functionality of the 2- wire interface is specified in the SFF-8436 specification.

The following Module and Channel digital diagnostic parameters are provided for monitoring:

- Transceiver Temperature
- Transceiver Supply Voltage

Also, the module micro-controller will generate an Interrupt Flag, by asserting the IntL signal, when an operational fault occurs. The host can identify the source of the interrupt by reading the appropriate registers through the 2-wire interface. The following Interrupt Flags are provided:

- Rx LOS - provided for each channel. This indicates that the optical power input into the receiver has dropped below a minimum allowed value.
- Tx Fault - provided for each channel. This indicates that a fault condition relating to either the laser, or one of the optical modulators, has occurred.
- Transceiver Temperature High and Low Alarm, and, High and Low Warning.
- Transceiver Supply Voltage High and Low Alarm, and, High and Low Warning.

SPECIFICATIONS

Electrical Characteristics

The QSFP AOC's maximum operating and storage conditions are shown in Table 1. Any stress beyond these maximum ratings may result in permanent damage to the device.

Table 1: Absolute Maximum Rating

Specifications	Symbol	Unit	Min	Max	Notes
Storage Temperature range	T_{sto}	°C	-40	85	
Powered case temperature	T_{case}	°C	0	70	Heat sink temperature
Operating Humidity	RH	%	5	90	Non-condensing
Supply voltage range	V_{CC1}	V	0.5	4.0	

Specifications listed in this documentation are only guaranteed when the QSFP AOC is operated under the recommended operating conditions listed in Table 2.

Table 2: Recommended Operating Conditions

Specifications	Symbol	Unit	Min	Max	Notes
Operating case temperature	T_{case}	°C	0	70	Heat sink temperature
Power supply voltage	V_{CC1}	V	3.15	3.45	
DC common mode voltage	V_{CM}	V	0	3.6	
Data rate		Gb/s	1	10.5	

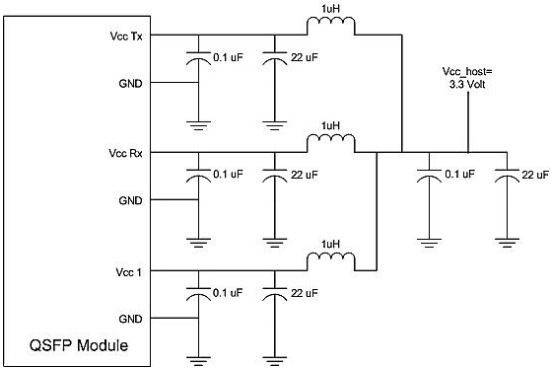
In addition to the recommended operating conditions, the power supply requirements are shown in Table 3.

Table 3: Power Supply Requirements

Specifications	Symbol	Unit	Min	Max	Notes
Power supply voltage	V_{CC1}	V	3.15	3.45	
Power supply current	I_{CC1}	mA	240 typical		
Power consumption		W		1.0	0.8W typical
Power supply noise including ripple		mV		50	1 kHz to frequency of operation measured at Vcc host

The QSFP+ specification recommends the use of a host board power supply filter to reduce power supply noise. The recommended power supply filter is shown in Figure 2.

Figure 2: QSFP+ Filtering Scheme



The QSFP AOC is designed to work with QSFP+ compliant sockets. The electrical requirements for input signal into the AOC are defined for the transmit side in Table 4 and for the receive side in Table 5.

Table 4: AOC Electrical Input Requirements

Specifications	Symbol	Unit	Min	Max	Notes
Data Rate Per Channel		Gb/s	0.001	10.5	
Differential Input Amplitude	V_{DI}	mV	150	1600	Peak to peak differential
Single Ended Voltage Tolerance		V	-0.3	3.8	
AC Common Mode Voltage		mV	15		RMS
Differential Input S-Parameter	SDD11	dB	See Note 1		10 MHz to 11.1 GHz
Reflected Differential to Common Mode Conversion	SCD11	dB		-10	10 MHz to 11.1 GHz
Total Jitter	TJ	UI_{p-p}		0.28	
Data Dependent Jitter	DDJ	UI_{p-p}		0.1	
Data Dependent Pulse Width Shrinkage	DDPWS	UI_{p-p}		0.055	
Uncorrelated Jitter	UJ	UI_{RMS}		0.023	
J2 Jitter Tolerance	J2	UI	0.17		
J9 Jitter Tolerance	J9	UI	0.29		
Eye Mask			See Note 2		Hit ratio = 5×10^{-5}

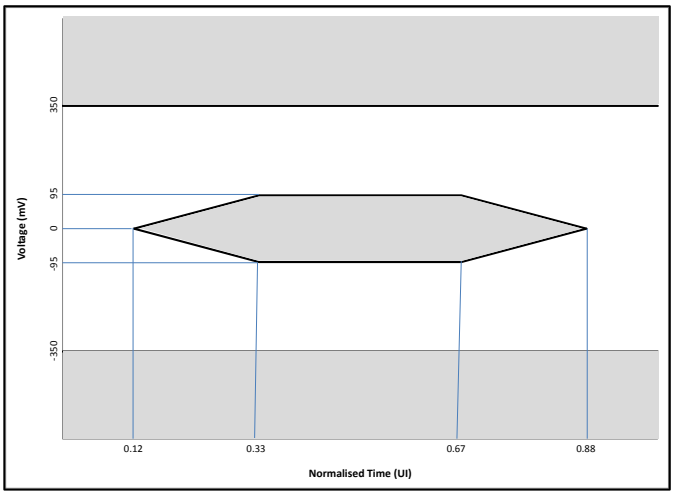
Notes for Table 4:

1 Maximum SDD11 is defined by the formulae:

$$0.1 < f < 4.11 \qquad -12 + 2\sqrt{f}$$

$$4.11 \leq f < 11.1 \qquad -6.3 + 13\log_{10}\left(\frac{5.5}{f}\right)$$

2 The worst case electrical input is defined by the eye mask:



Specifications	Symbol	Unit	Min	Max	Notes
Data Rate Per Channel		Gb/s	0.001	10.3125	
Termination Mismatch at 1MHz	ΔZ_M	%		15	
Output AC Common Mode Voltage		mV		7.5	RMS
Single Ended Output Voltage Tolerance		V	-0.3	3.8	
Differential Output Amplitude	V_{DO}	mV	340	700	Peak to peak differential
Differential Output Amplitude in squelched state		mV		50	Peak to peak differential
Differential Unsigned Amplitude	V_{diffc}		0.1	0.6	
Common Mode Output Reflection Coefficient	SCC22	dB	See Note 1		10 MHz to 11.1 GHz
Differential Output S-Parameter	SDD22	dB	See Note 2		10 MHz to 11.1 GHz
Output Transition Time	Tr, Tf	ps	28		20% to 80%
Skew Between Channels		ns		5	
Total Jitter	TJ	UI_{p-p}		0.7	
Deterministic Jitter	DJ	UI		0.4	
J2 Jitter		UI_{p-p}		0.42	
J9 Jitter		UI_{p-p}		0.65	
Eye Mask			See Note 3		Hit ratio = 5×10^{-5}
Eye Mask			See Note 3		Hit ratio = 1×10^{-12}

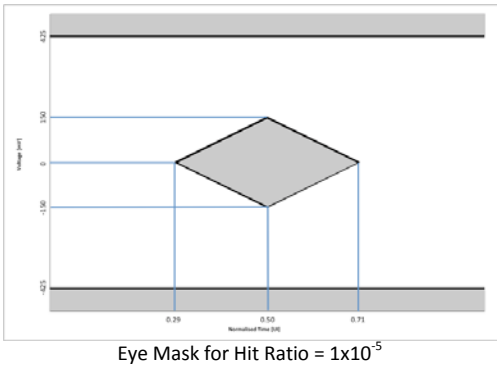
1 Maximum SCC22 is defined by the formulae:

0.1 < f < 2.5	$-7 + 1.6f$
2.5 ≤ f <11.1	-3

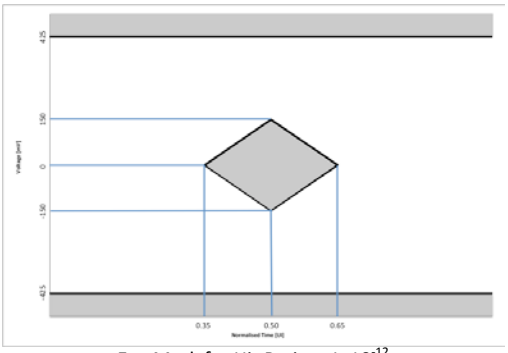
2 Maximum SDD22 is defined by the formulae:

0.1 < f < 4.11	$-12 + 2\sqrt{f}$
4.11 ≤ f <11.1	$-6.3 + 13\log_{10}\left(\frac{5.5}{f}\right)$

3 Two eye masks are specified, but are considered to be identical due to the differences in the hit ratio:



Eye Mask for Hit Ratio = 1×10^{-5}



Eye Mask for Hit Ratio = 1×10^{-12}

Interfaces

Control Interface

As described in the QSFP standard, the electrical interface has the following low speed signals for control and status: ModSelL, LPMode, ResetL, ModPrsL, IntL. Their operation is described below:

ModSelL	The ModSelL signal allows multiple QSFP+ modules to be on a standard I^2C serial control bus. By default, this pin is held low by the host. In this state, the module will respond to the I^2C interface. When the ModSelL pin is pulled high by the host, the module will not respond to or acknowledge any I2C query or command. Care must be taken to ensure that if the ModSelL pin is used to toggle control of different modules, the assert and deassert times must be taken into account to prevent communication conflicts.
LPMode	The LPMode pin is used by the host to set the maximum power consumption by the module. This is intended to protect hosts that are not designed to cool higher power modules that draw more than 1.5W. Since the power consumption of QSFPO-40G AOC is 0.8W maximum, this pin is not used and the module is always in a low power state.
ResetL	The AOC can be reset to its default settings by pulling this control pin to a low level for a period longer than the minimum pulse length of the 2-wire serial interface. Whilst in this reset state, host should disregard all status bits.
ModPrsL	ModPrSL is used to indicate to the host that the connector is populated by the AOC. In the absence of an AOC, this is pulled up to the host Vcc. When the AOC is inserted, it completes the path to ground through a resistor on the host and pulls ModPrsL to a low state.
IntL	This control pin is used to indicate a possible module operation fault or a status critical to the host system. The IntL pin is an open collector output ad must be pulled to the Host Vcc voltage on the Host board. When pulled “low” by the AOC, the alarm is active and the AOC will identify the source of the interrupt using the 2-wire serial interface.

In addition, there is an industry standard two wire serial interface scaled for 3.3 volt LVTTL. It is implemented as a slave device. Signal and timing characteristics are further defined in the Section 0, below and also Section 0.

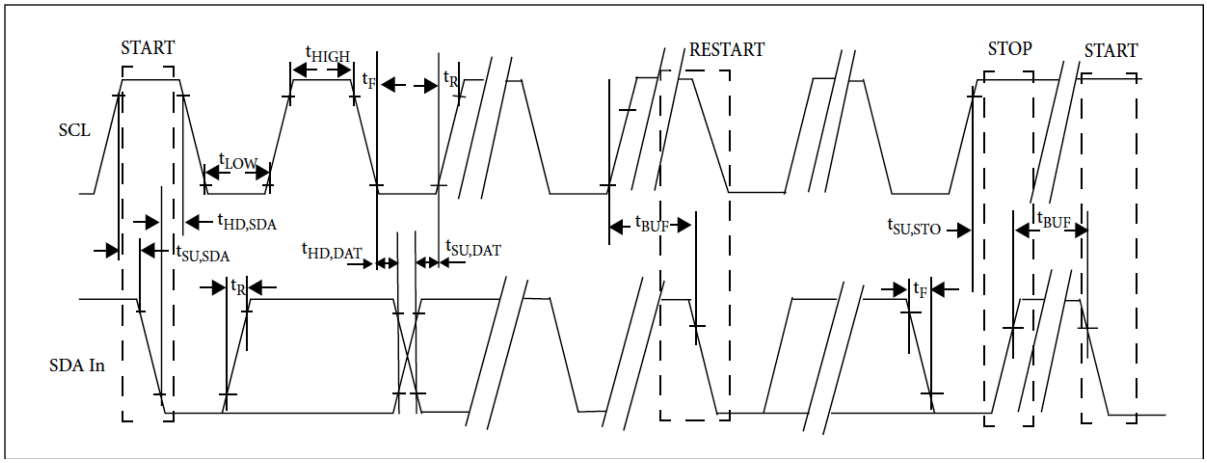
2-Wire Serial Interface

Table 5 and Figure 3 show the 2-wire timing specifications as defined by SFF-8436. Table 4

Table 5: Optical Engine 2-wire Timing Specifications

Parameter	Symbol	Unit	Min	Typ	Max	Conditions
Clock Frequency	f_{SCL}	KHz	0	400	400	
Clock Pulse Width Low	t_{LOW}	µs	1.3			
Clock Pulse Width High	t_{HIGH}	µs	0.6			
Time bus free before new transmission can start	t_{BUF}	µs	20			Between STOP and START
START Hold Time	$t_{HD,STA}$	µs	0.6			
START Set-up Time	$t_{SU,STA}$	µs	0.6			
Data In Hold Time	$t_{HD,DAT}$	us	0			
Data In Set-up Time	$t_{SU,DAT}$	µs	0.1			
Input Rise Time (400kHz)	$t_{R,400}$	ns			300	From $V_{IL,MAX}$-0.15 to $V_{IH,MIN}$ + 0.15
Input Fall Time (400kHz)	$t_{F,400}$	ns			300	From $V_{IL,MAX}$-0.15 to $V_{IH,MIN}$ + 0.15
STOP Set-up Time	$t_{SU,STO}$	µs	0.6			
ModSelL Setup Time	HOST_select_setup	ms	2			Setup time on the select lines before start of a host initiated serial bus sequence
ModSelL Hold Time	Host_select_hold	µs	10			Delay from completion of a serial bus sequence to changes of module select status
Abort Sequence – Bus Release	Deselect_abort	ms	2			Delay from a host de-asserting ModSelL (at any point in a bus sequence), to the module releasing SCL and SDA

Figure 3: 2-Wire Timing Diagram (per SFF-8436)



Control, Status and Monitor Interface

Table 7 and Table 8 provide the specifications of the control, status and monitoring interface.

Table 7: I/O Timing for Control, Status and Monitoring

Specifications	Symbol	Unit	Min	Max	Notes
Initialization time	t_{INIT}	ms		2000	Time from power on, hot plug or rising edge of reset until the module is fully functional.
Reset init assert time	t_{RESET_INIT}	µs		2.5	A reset is generated by a low level longer than the minimum reset pulse time present on the ResetL pin
Serial bus hardware ready	t_{SERIAL}	ms		2000	Time from power on 2 until module responds to data transmission over the 2-wire serial bus
Monitor data ready time	t_{DATA}	ms		2000	Time from power on2 to data not ready, bit 0 of Byte 2, de-asserted and IntL asserted
Reset assert time	t_{RESET}	ms		2000	Time from rising edge on the ResetL pin until the module is fully functional[3]
IntL assert time	t_{ON_INTL}	ms		200	Time from occurrence of condition triggering IntL until Vout:IntL = Vol
IntL de-assert time	t_{OFF_INTL}	µs		500	Time from clear on read[4] operation of associated flag until Vout:IntL = Voh. This includes de-assert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS assert time	t_{ON_LOS}	ms		100	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted
Tx fault assert time	$t_{ON\_TXFAULT}$	ms		200	Time from Tx Fault state to Tx Fault bit set (value = 1b) and IntL asserted
Flag assert time	t_{ON_FLAG}	ms		200	Time from occurrence of condition triggering flag to associated flag bit set (value = 1b) and IntL asserted
Mask assert time	t_{ON_MASK}	ms		100	Time from mask bit set (value = 1b)[1] until associated IntL assertion is inhibited
Mask de-assert time	t_{OFF_MASK}	ms		100	Time from mask bit cleared (value = 0b)[1] until associated IntlL operation resumes
Application or rate select change time	t_{RATE_SEL}	ms		100	Time from change of state of Application or Rate Select bit[1] until transmitter or receiver bandwidth is in conformance with appropriate specification
Power over-ride or power set assert time	t_{ON_PDOWN}	ms		100	Time from P_Down bit set (value = 1b)1 until module power consumption enters Power Level[1]
Power over-ride or power set de-assert time	t_{OFF_PDOWN}	ms		300	Time from P_Down bit cleared (value = 0b)[1] until the module is fully functional[3]

Note 1. Measured from falling clock edge after stop bit of write transaction
Note 2. Power is defined as the instant when supply voltages reach and remain at or above the minimum level specified in Table 3
Note 3. Fully functional is defined as IntL asserted due to data not ready bit, bit 0 byte 2 de-asserted. The module should also meet electrical specifications.
Note 4. Measured from falling edge after stop bit of read transaction.

Table 8: I/O Timing for Squelch

Specifications	Symbol	Unit	Min	Max	Notes
Rx squelch assert time	t_{ON_RXSQ}	µs		80	Time from loss of Rx input signal until the squelched output condition is reached.
Rx squelch de-assert time	t_{OFF_RXSQ}	µs		80	Time from resumption of Rx input signals until normal Rx output condition is reached.

INITILIZATION PROCEDURE

Memory Map

Introduction – EEPROM Virtual Addressing

The SFF-8436 specification calls for a list of cable parameters to be readable through an I2C interface, commonly referred as the "EEPROM" parameters. When the first standard revision was written, all the parameters were static, and they were actually stored in an on-board EEPROM. As revisions evolved, some of the fields became dynamic (such as temperature or optical power readings), while others (such as interrupts and alarms) became Read/Write (R/W). As a result, an EEPROM based implementation did not suffice anymore, although the term is still used to refer to the Memory Map. We will refer to this as the "SFF Memory Map".

Consequently, the Samtec current implementation, although referred to as an "EEPROM map", does not using an actual direct EEPROM read or write. Instead, each I2C read or write request is interpreted by the embedded microprocessor in the optical engine. The microprocessor then reads or stores data which could come from / go to different sources:

- The processor's own internal EEPROM
- The processor's static, dynamic RAM or register memory
- Sensors or internal chipset readings
- Internal processor calculations or registers

An important consequence is that EEPROM byte addresses used in I2C requests are virtual – they will not always correspond to the physical address in the processor internal EEPROM, or might not have a physical EEPROM location at all.
This is invisible to the end user, who just reads and writes to the I2C as if it were an actual EEPROM according to the standard SFF memory map. The processor will take care of fetching and writing the data internally from/to the correct physical location.

Instructions for modifying the EEPROM map can be found in Section 0.

SFF Memory Map

The structure of the SFF Memory Map as defined by SFF-8436 rev. 3.8 is shown in Figure 3.

For historical reasons, the SFF memory map is somewhat contrived. It is divided into lower and upper memory:
The lower memory is a block or “page” of 128 bytes, and its bytes address are numbered 0 to 127.
The upper memory is itself divided in four pages, numbered page 0 to page 3 Each Page is also 128 bytes long block, but with byte addresses numbered 128-255 for each page.

All QSFP+ are hard-wired at I2C device address A0h. The lower page is accessed by using the A0h address as device address, and the 0 to 127 address as the byte address.
Upper pages are accessed by first writing the desired page number at byte in address 127 (Page Select Byte). Any subsequent byte read or write request in the address range 128-255 will be done from/to the page that has been specified in the Page Select Byte. Samtec AOCs do not use Page 02

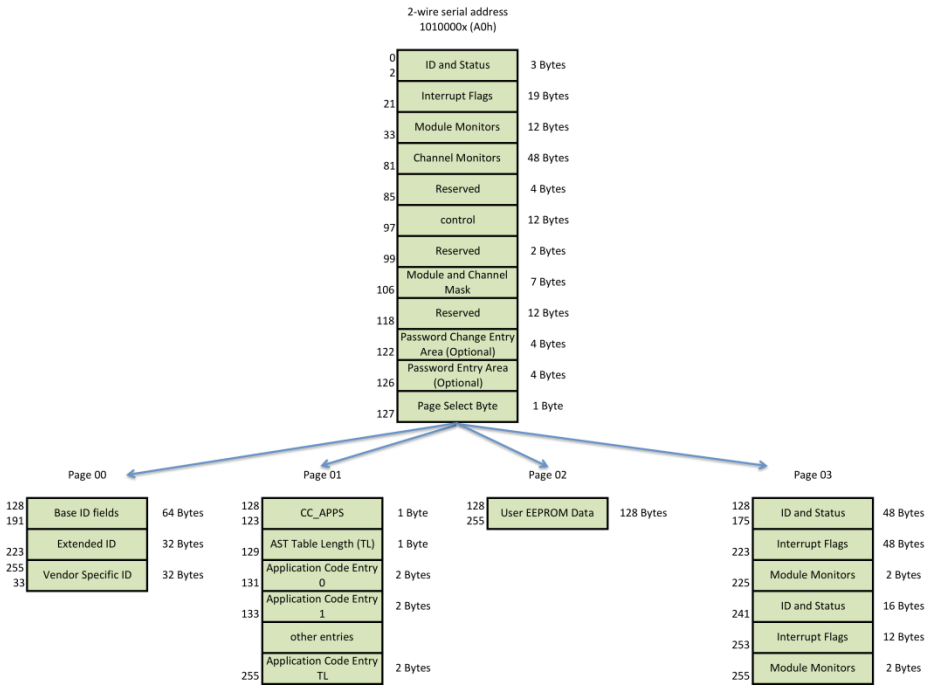


Figure 3: Structure of the SFF Memory Map (from the SFF specification)

Below is a summary description of the memory pages. For more details, see pages 16-18 of this product specification:

- Lower memory, Page 00, bytes 0-127: contains status, interrupt and monitoring information.
- Page 00, bytes 128-255: contains standardized Read-Only information for the end-user. The data is physically mapped to the microprocessor internal EEPROM bytes 128-255.
- Page 01, bytes 128-255 is optional and not supported in the Samtec AOC.
- Page 02, bytes 128-255 is available for the user to store and read his own data.
- Page 03, bytes 128-255 contains module thresholds, channel thresholds and masks, and optional channel controls.

Page 00, Lower Memory

Many of the lower memory bytes are optional or not applicable to an AOC implementation. Table 6 lists the bytes and corresponding features supported in our implementation. Full details about the bit fields and usage can be found in the SFF-8436 specification.

Table 6: Supported Page 00 Lower Memory Fields

Page 00 Byte #	Description	Default Value	Read-only / Read-Write	Notes
0	Identifier	OD	RO	
2	Status – Flat or paged memory	0	RO	
3	Interrupt Flags – LOS		R0	1
4	Interrupt Flags – Tx Fault		RO	
6	Interrupt Flags – Temp Alarm		RO	
7	Interrupt Flags – Voltage Alarm		RO	
22	Module Monitors – Temperature MSB		RO	
23	Module Monitors – Temperature LSB		RO	
26	Module Monitors – Supply Voltage MSB		RO	
27	Module Monitors – Supply Voltage LSB		RO	
86	Control – Transmitter Disable		R/W	
93	Low Power Control		R/W	2
100	Interrupt Masks – Tx LOS Mask	0	R/W	
101	Interrupt Mask s – Tx Fault Mask	0	R/W	
103	Interrupt Masks – Temperature Fault Mask	0	R/W	
104	Interrupt Masks – Voltage Fault Mask	0	R/W	
119	Password Change Entry Data		R/W	3
120	Password Change Entry Data		R/W	3
121	Password Change Entry Data		R/W	3
122	Password Change Entry Data		R/W	3
123	Password Entry Area		R/W	3
124	Password Entry Area		R/W	3
125	Password Entry Area		R/W	3
126	Password Entry Area		R/W	3
127	Page Select Byte		R/W	

[1] *Rx only. Tx LOS not supported*
[2] *The engine always runs in low power mode, writing to this register has no effect*
[3] *User settable password protection of page 02 not supported*

Page 00, Upper Memory

The values for the Page 00 Upper Memory bytes are shown in Table. Default factory-programmed values for Infiniband are shown. Fields that are adjusted at manufacturing time are bolded. Please contact Samtec for alternate default configurations.

Table 10: Page 00 Upper Memory Fields (factory default, Infiniband)

Byte #	Bit(s)	Description	Value	Notes
128	7:0	Identifier	0Dh	
129	7:6	Extended identifier values, power class	00	Power Class 1 Module (1.5W max)
130	7:0	Connector	23h	AOC has no optical connector
140	7:0	Nominal BR	64h	Nominal Bit Rate = 10,000 Mbs
142	7:0	Cable length (SM fiber)	0	Not Applicable
143	7:0	Cable length (OM3 fiber)	0	Not Applicable
144	7:0	Cable length (OM2 fiber)	0	Not Applicable
145	7:0	Cable length (OM1 fiber)	0	Not Applicable
146	7:0	Link length for copper or active cable	*	Cable Dependent, units of 1m
147	7:4	Transmitter technology	0000	850 nm VCSEL
148-163		Vendor name	Samtec Inc	
164	3:0	Extended module codes (InfiniBand data rates)	00111b	SDR, DDR & QDR
165-167		Vendor OUI	04C880h	
168-183		Vendor part number	QSFPO	
184-185		Vendor revision	0	
186	7:0	wavelength (fiber)	42h	Wavelength = 850nm
187	7:0	wavelength (fiber)	68h	Wavelength = 850nm
188	7:0	wavelength tolerance	0Fh	Wavelength Tolerance = 20nm
189	7:0	wavelength tolerance	A0h	Wavelength Tolerance = 20nm
190	7:0	Max case temp	70	Max Temp Case = 70C
191	7:0	Check sum	178	Recalculated checksum
193	0	RX output amplitude programming	0	Not Implemented
194	3	RX squelch disable implemented	0	Not Implemented
194	2	RX output disable capable	1	RX output disable capable
194	1	TX squelch disable implemented	0	Not Implemented
194	0	TX squelch implemented	0	Not Implemented
195	7	Memory page 02 provided	1	Memory Provided
195	6	Memory page 01 provided	0	Not Implemented
195	4	TX disable implemented (also disables serial output)	1	TX disable implemented
195	3	TX fault reporting implemented	1	TX fault reporting implemented
195	1	LOS and reporting implemented	0	Not Implemented
196-211	All	Vendor serial number	**********	Cable Dependent
212-217	All	Date code	******	YYMMDD
218-219	All	Lot code	00	Optional
223	7:0	Check sum	42	Recalculated checksum
224-255	All	Vendor specific information	FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF0001 10	

Notes to Page 00 Implementation

Please see Table 11 for further clarifications of our implementation some Page 00 fields.

Table 11: Notes to the Memory Map Implementation

Type of Parameter	Address		Name	Notes
	Page	Byte		
Interrupt flag	00	3	Tx_LOS	Not Provided
Interrupt Flag	00	9-10	L-Rx Power Alarm	Not Provided
Channel Monitoring	00	34-41	Rx Input Power	Rx input power is not supported
Channel Monitoring	00	42-49	Tx Bias	Tx bias monitoring is not supported
Channel Mask	00	100[7:4]	M-Tx LOS	Tx LOS is not supported
Optional Channel Controls	03	241[3:0]	Tx SQ Disable	Tx squelch is not supported

Page 02

Page 02, bytes 128-255 are provided for end-customer own use. The fields are initialized to 0 at the factory.

Page 03

Table 7: Supported Page 03 Fields

Page 03 Byte #	Description	Default Value	Read-only / Read-Write
128	Temp High Alarm MSB	75C	R
129	Temp High Alarm LSB		R
130	Temp Low Alarm MSB	0C	R
131	Temp Low Alarm LSB		R
132	Temp High Warning MSB	70C	R
133	Temp High Warning LSB		R
134	Temp Low Warning MSB	5C	R
135	Temp Low Warning LSB		R
144	Vcc High Alarm MSB	3.465V	R
145	Vcc High Alarm LSB		R
146	Vcc Low Alarm MSB	3.135V	R
147	Vcc Low Alarm LSB		R
148	Vcc High Warning MSB	3.3825V	R
149	Vcc High Warning LSB		R
150	Vcc Low Warning MSB	3.2175V	R
151	Vcc Low Warning LSB		R
176	Rx Power High Alarm MSB		R
177	Rx Power High Alarm LSB		R
240	Squelch Disable		R/W
241	Rx Output Disable		R/W

Output Voltage and Pre-emphasis Settings

The Rx output amplitude swing and pre-emphasis is factory adjustable. Please contact Samtec if amplitude and pre-emphasis values other than the default values are required.

It is typically not recommended to change the default values. However, some reasons for requesting factory adjustment of these parameters are:

Permanently disabling one or more channels
adjusting pre-emphasis and output swing for communication over non-standard or difficult electrical channels
reducing output swing and pre-emphasis for power savings with well-behaved channels.

Four output voltages amplitudes settings are available

0 mV (Rx channel permanently disabled)
317 mV
422 mV (factory default)
739 mV

Four pre-emphasis settings are available:

0 mV
125 mV (factory default)
175 mV
325 mV

Figure 4 and Figure 5 show typical received eyes for some combinations of amplitude and pre-emphasis settings. The engines are shipped by default with 422mV amplitude / 125 mV pre-emphasis settings – these are highlighted.
In addition to changing the output eye, changing these settings also affect the power consumption of the optical engine as shown on Table 13. Reducing voltage and pre-emphasis results in the lowest power consumption available, while larger voltage and pre-emphasis might be used in special non-standard applications to overcome poor electrical traces or provide more design margin at the expense of power consumption.

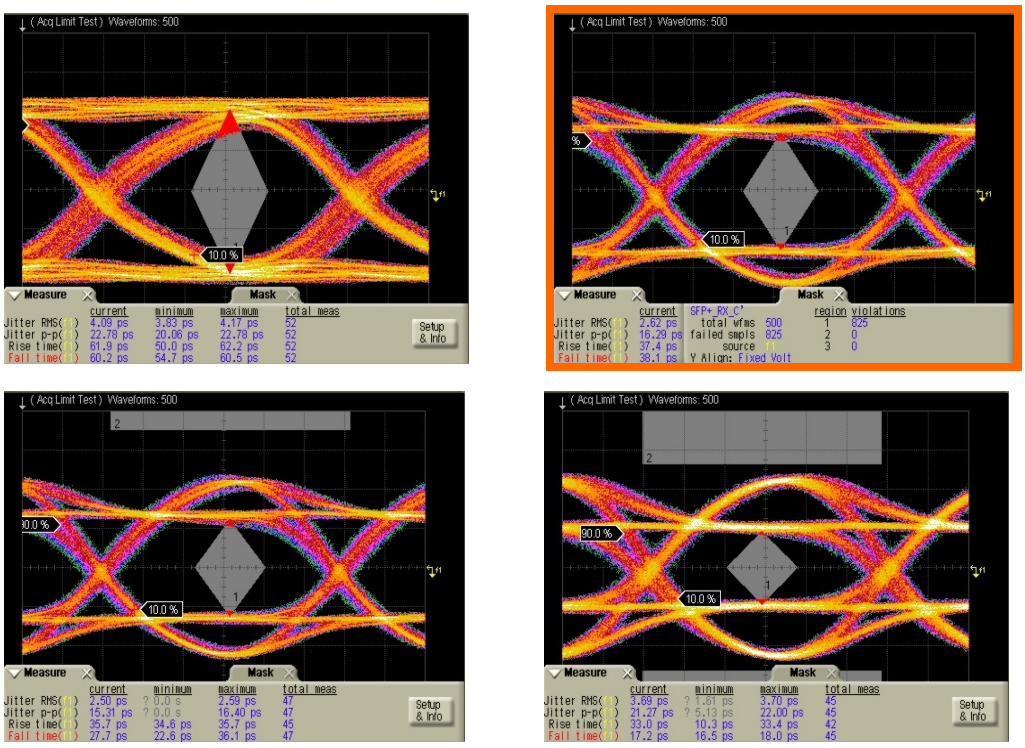


Figure 4: Typical output eyes, 422 mV amplitude settings
Top: 0 and 125 mV pre-emphasis, Bottom: 175 and 325 mV pre-emphasis

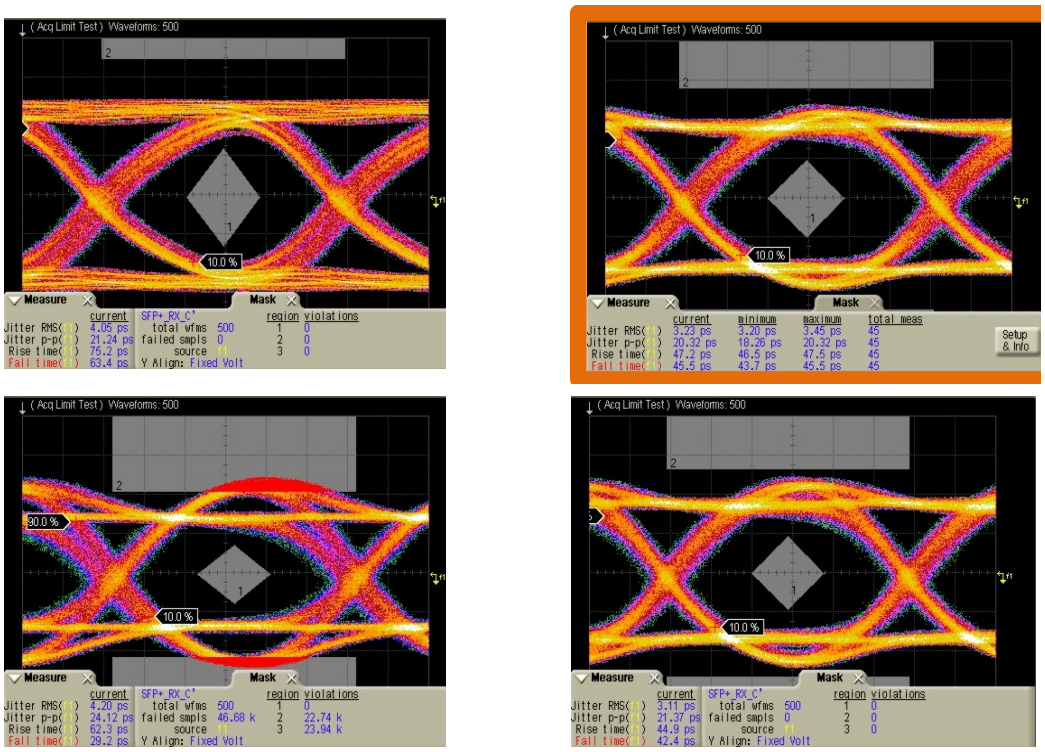


Figure 5: Typical output eyes, 739 mV amplitude settings
Top: 0 and 125 mV pre-emphasis, Bottom: 175 and 325 mV pre-emphasis

Table 13: Typical Power Consumption vs. Rx settings

Rx Output Voltage Swing Setting (mV)	Rx Output Pre-emphasis Setting (mV)	Typical Power Consumption (mW)	Notes
317	0	590	
317	125	740	
317	175	770	
317	325	850	
422	0	620	
422	125	770	Default Settings
422	175	800	
422	325	890	
739	0	710	
739	125	860	
739	175	890	
739	325	980	

The assemblies are shipped by default with 422mV amplitude / 125 mV pre-emphasis settings and lead to a 770 mW typical power dissipations. Please contact Samtec if other defaults are desired.

MODIFYING THE MEMORY MAP AND INTERNAL SETTINGS

A Windows based utility is available to edit the QSFPO-40G memory map values as well as modify and read various factory-only internal settings. This software utility is called, QSFPsende.exe.

Software Tool and Hardware Requirements

The following are required to run the QSFPSend application

Windows computer

Total Phase Aardvark I2C/SCPI Interface (TP240141)[1]

http://www.totalphase.com/products/aardvark_i2cspi/

Total Phase 10-pin split cable (TP249212 or TP240411)

http://www.totalphase.com/categories/accessory/

3.3V power supply

Programming cable connecting the QSFP AOC edge connector to the power supply and Aardvark. This test cable should be wired as in Figure 4.

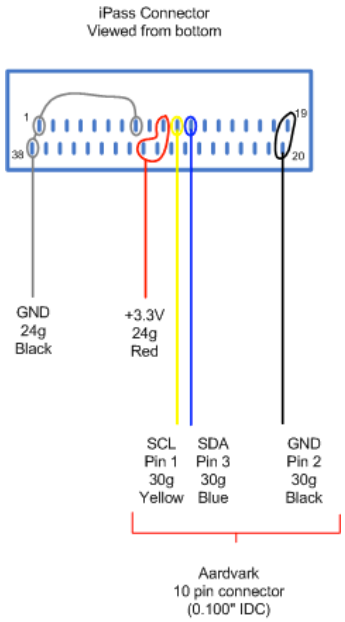


Figure 4: QSFP programming cable

[1] At this time, the Aardvark USB to I2C interface is the only supported hardware device for accessing the I2C bus via the QSFPsend utility.

Installing and Connecting the Hardware

Install the Aardvark software per manufacturer instructions.

Connect the USB side of the Aardvark to the USB port of the computer
Connect the data side of the breakout cable to the I2C outputs of the Aardvark
Connect the 3.3V power supply to the power input in the breakout cable
Connect the QSFPO-40G AOC to the QSFP end of the breakout cable

Your setup should be as in Figure 5.

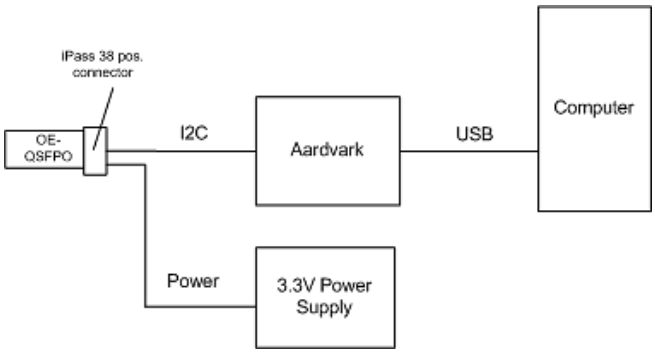


Figure 5: QSFPO-40G Programming Setup

Installing and Running the QSFPsend Utility

Copy the QSFPsend.exe program and the examples .csv command files to an easily accessible location on your hard disk (the following example assumes they are put in C:\Test\)

QSFPsend.exe is a simple command line program to read and write QSFP mapped registers and the internal EEPROM used to control the device. It is run by typing a command looking generically like

QSFPsend <filename>

Where **<filename.csv>** is a comma delimited file containing the data to be read or edited in the memory map. Detail of the syntax of the CSV files and common examples are given below. Example .csv files are provided with the software.

Open a command window (go to start, run…, type “cmd”). Navigate to the directory where you installed by typing:

cd C:\Test

Type the following command:

QSFPsend ReadVendorPN.csv

You should get the following output reading the part number field.

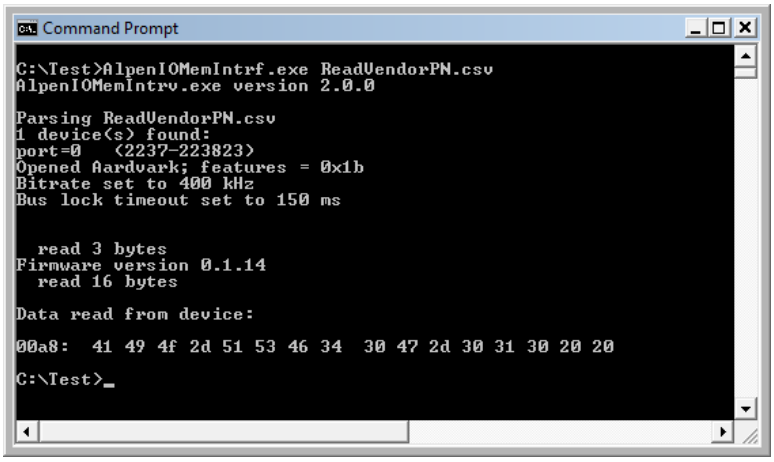

Command Prompt
C:\Test>AlpenIOMemIntrf.exe ReadVendorPN.csv
AlpenIOMemIntrv.exe version 2.0.0
Parsing ReadVendorPN.csv
1 device(s) found:
port=0 (2237-223823)
Opened Aardvark; features = 0x1b
Bitrate set to 400 kHz
Bus lock timeout set to 150 ms
read 3 bytes
Firmware version 0.1.14
read 16 bytes
Data read from device:
00a8: 41 49 4f 2d 51 53 46 34 30 47 2d 30 31 30 20 20
C:\Test>

Figure 6: Sample Output from QSFPsend

Note that the QSFP's firmware version must be version 0.1.14 or higher to read and write the EEPROM using QSFPsend. When QSFPsend is run, it outputs the firmware version as shown in Figure 6.

Syntax

The tool is launched by command line and takes a .csv data file as its argument, using the following syntax:

WSFPsend [-l] [-r] [-c] filename.csv

Parameters

-l	Used only for reads. Prints in long form where every read byte resides on its own line. This allows the parameters to be easily saved in a .csv file.
-r	Used only for writes. Reads back the registers that were just written.
-c	Used for both read and writes. Calculates the 2 check sums on Page00 and writes them to their proper locations in EEPROM even if Page00 was not accessed.
filename.csv	A comma delineated file detailing the parameters to read or write. The format of this field is described below.

Common Examples

The following are examples of .csv files to perform the most common tasks (each example starts with '#' describing the action to be performed and consists of 3-18 lines):

#set Cable Length to 10m
16,ab,94
0a

#set Vendor Name to 'Samtec Inc. '
16,ab,92
0a
61
6d
74
65
63
20
49
6e
63
2e
20
20
20
20
20

#set Vendor OUI to '04c880h'
16,ab,a5
04
C8
80

#set Cable Part Number to '1234567890 '
16,ab,a8
31
32
33
34
35
36
37
38
39
30
20
20
20
20
20
20
20

#set Part Number Revision to ‘-1’
16,ab,a8
2d
31

#set Cable Serial Number to ‘0246813579 ’
16,ab,c4
30
32
34
36
38
31
33
35
37
39
20
20
20
20
20
20

#set Date Code to 4July2011
16,ab,d4
31
31
30
37
30
34

#set Lot Code to ‘01’
16,ab,da
30
31

#set Output Amplitude=422mV and pre-emphasis=125mV
16,ab,6
00
55

INTERFACE

Electrical

Figure 6 shows the contact numbering for the assembly connector. The diagram shows the module from the bottom view. There are 38 pins intended for high speed low speed signals, power and ground connections. These pins are described in Table 8.

Pin	Logic	Symbol	Description	Plug Sequence	Note
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTLL-I	ModSelL	Module Select	3	
9	LVTLL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2 wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2 wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTLL-O	ModPrsL	Module Present	3	
28	LVTLL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTLL-I	LPMode	Low Power mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	T1xn	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1
Note 1. GND is the symbol for signal and supply (power) common for the Optical Engine. All are common within the Optical Engine and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.					
Note 2. Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 3. The connector pins are each rated for a maximum current of 500mA.					

Table 8: Edge Connector Pin Descriptions

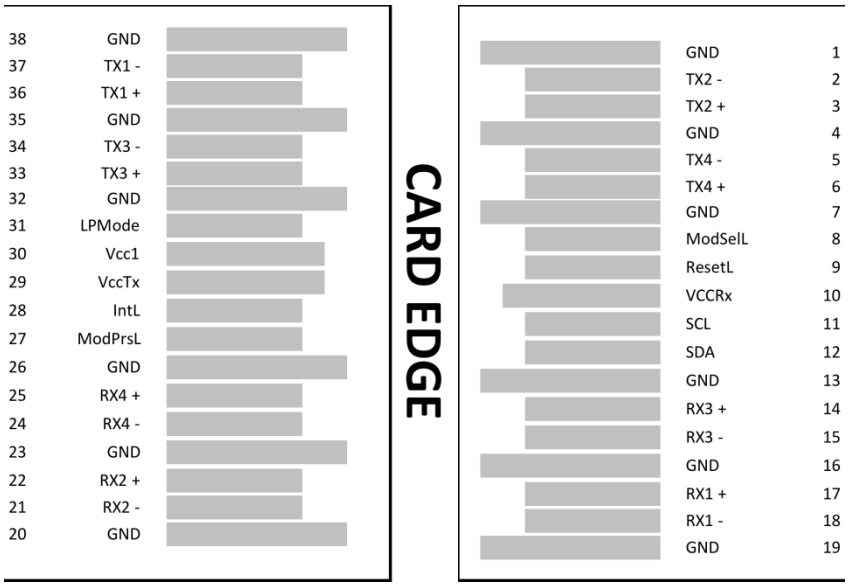


Figure 6: Edge Connector Pinout

MECHANICAL CHARACTERISTICS

Connector Dimensions

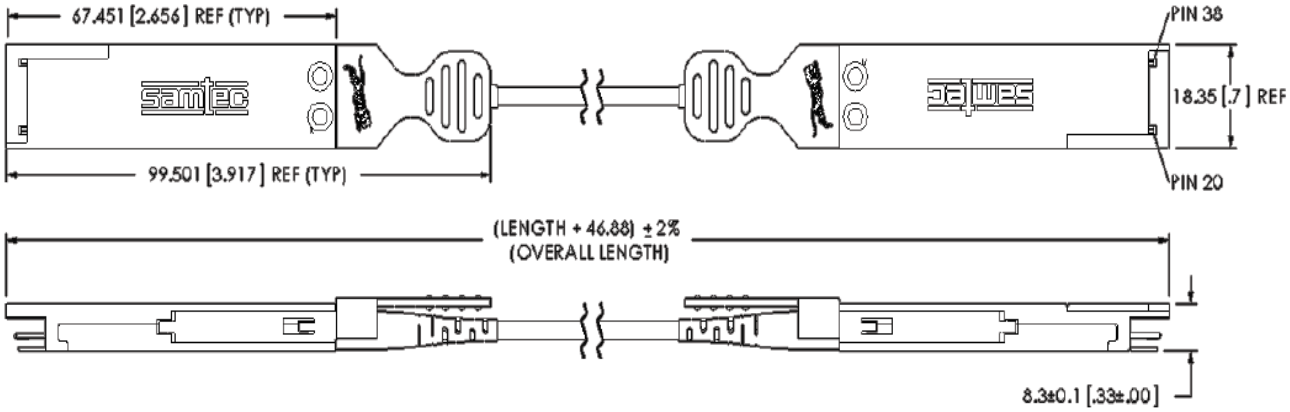


Figure 7: Connector Dimensions

TECHNICAL INFORMATION

Regulatory & Compliance

Table 15: Regulatory and Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the electrical contact	JEDEC Human Body Model (HBM) (JESD22-A114-B) JEDEC Machine Model (MM) (JESD22-A115-A)	1kV TBD
Electrostatic Discharge (ESD) to module case	Variation of IEC 61000-4-2	15kV
Electromagnetic Interference (EMI)	FCC part 15 CENELEC EN55022 (CISPR 22A) VCCI class1	TBD
EMI Immunity	Variation of IEC 61000-4-3	10V/m, 80 – 1000Mz
Laser eye safety	IEC 60825-1 amendment 2 CFR 21 section 1040	Class 1M
RoHS compliance	RoHS 6/6 directive 2002/95/EC amendment 4054 (2005/747/EC)	

Ordering Information and Technical Support

Part Number: QSFPO-40G-XXX.X-XX

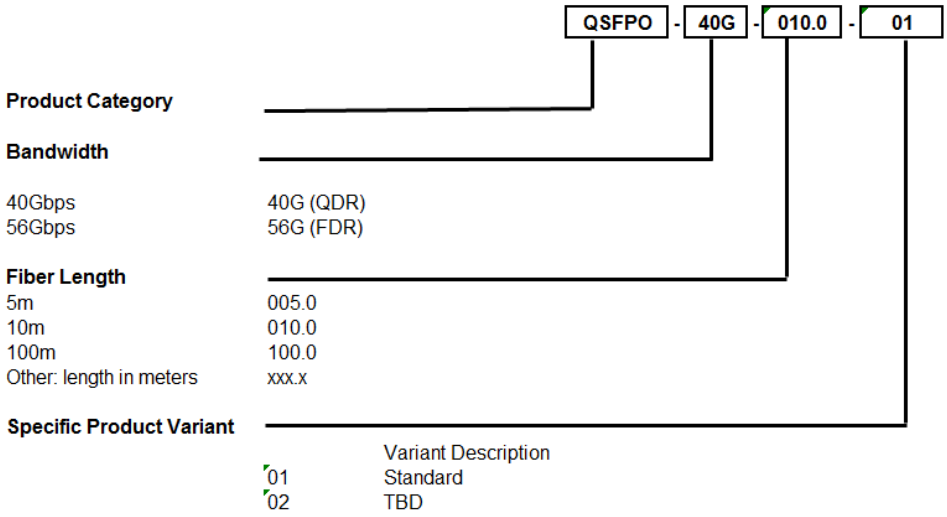


Figure 8: QSFPO-40G AOC Part Numbering

Contact Samtec for Sales or Technical support.

1-800-SAMTEC-9
Optical Sales: (408) 406-4123
Technical Support: (302) 521-7798

Definitions

This document uses the following conditions:
All voltages are referred to GND unless otherwise specifically noted.
Currents are defined positive out of the pin.

Reference Documents

SFF-8436: QSFP specifications document
SFF-8431: SFF specifications document

Please see http://www.sffcommittee.org/ie/Specifications.html for the most recent versions of these documents.

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Revision History

Table 16: Revision History

Date	Rev. No.	Status	Comments	Author	Approver
12/14/2009	001	Draft	Initial Draft	ME	
10/24/2010	002	Release	Preliminary Release	MV	
06/20/2011	003	Release	New EEPROM section	MV	
07/08/2011	004	Release	Update all sections	MV/BT	
07/28/2011	005	Release	EEPROM Programming, new part number	MV/BT	
01/05/2012	1.0	Draft	QSFPO-40G AOC Revision	MA	
06/01/2012	1.1	Release	Conversion to Samtec format	KB	

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